

What is claimed is:

- 1 1. A method comprising:  
2 receiving video into a video display device;  
3 storing, by at least one processor, the video into a memory, upon  
4 determining that the video display device is in a storage mode; and  
5 performing enhanced image processing on the video with the at least one  
6 processor, upon determining that the video display device is in an image processing  
7 mode.
- 1 2. The method of claim 1, further comprising compressing, by the at least one  
2 processor, the video prior to storing the video into the memory, upon determining  
3 that the video display device is within the storage mode.
- 1 3. The method of claim 2, wherein compressing, by the at least one processor,  
2 the video comprises performing frame reduction on the video, by a first processor of  
3 the at least one processor.
- 1 4. The method of claim 3, wherein compressing, by the at least one processor,  
2 the video comprises scaling, by a second processor of the at least one processor, of  
3 the video.
- 1 5. The method of claim 1, wherein performing enhanced image processing on  
2 the video comprises performing a ghost reduction operation.
- 1 6. The method of claim 1, wherein performing enhanced image processing on  
2 the video comprises performing a noise reduction operation.
- 1 7. The method of claim 1, wherein performing enhanced image processing on  
2 the video with the at least one processor comprises performing a first enhanced

3 image processing operation on the video with a first processor of the at least one  
4 processor and performing a second enhanced image processing operation on the  
5 video with a second processor of the at least one processor.

1 8. The method of claim 7, further comprising transmitting output of the first  
2 enhanced image processing operation from the first processor to the second  
3 processor through a logical connection that includes a path through a third  
4 processor, wherein the third processor is not configured to perform a process  
5 operation on the output as part of the transmitting of the output through the logical  
6 connection.

1 9. An apparatus comprising:  
2 an input/output interface coupled to a memory; and  
3 a first programmable processor to perform a first enhanced image processing  
4 operation on video if a current mode of the apparatus is an image processing mode,  
5 and wherein the first programmable processor is to store the video into the memory  
6 if the current mode of the apparatus is a storage mode.

1 10. The apparatus of claim 9, further comprising a second programmable  
2 processor to perform a second enhanced image processing operation on the video if  
3 the current mode of the apparatus is the image processing mode, and wherein the  
4 second processor is to perform a video compression operation to the video prior to  
5 storage of the video into the memory if the current mode of the apparatus is a  
6 storage mode.

1 11. The apparatus of claim 10, wherein the video compression operation is  
2 selected from a group consisting of an image scale operation and a frame rate  
3 reduction operation.

1 12. The apparatus of claim 10, further comprising a third programmable  
2 processor to perform a third enhanced image processing operation on the video if  
3 the current mode of the apparatus is the image processing mode, and wherein the  
4 third processor is to perform a noise reduction operation on the video prior to the  
5 video compression operation if the current mode of the apparatus is the storage  
6 mode.

1 13. The apparatus of claim 9, further comprising a host processor to receive  
2 control input from a user of a video display device that includes the apparatus,  
3 wherein the control input is to cause a change in the current mode, wherein the host  
4 processor is to update microcode in the first programmable processor if the control  
5 input is to cause a change from the current mode.

1 14. An apparatus comprising:  
2 a memory;  
3 a first programmable processor to perform a first enhanced image processing  
4 operation on video if a current mode of the apparatus is an image processing mode,  
5 and wherein the first programmable processor is to perform a compression operation  
6 on the video if the current mode of the apparatus is a storage mode; and  
7 a second programmable processor to receive output from the first enhanced  
8 image processing operation through a first logical connection that includes a path  
9 through a third programmable processor and to perform a second enhanced image  
10 processing operation on the video if the current mode of the apparatus is the image  
11 processing mode, and wherein the second programmable processor is to receive  
12 output from the compression operation through a second logical connection that  
13 includes a path through a fourth programmable processor and to store the video into  
14 the memory if the current mode of the apparatus is the storage mode.

1 15. The apparatus of claim 14, further comprising a host processor to receive  
2 control input from a user of a video display device that includes the apparatus,

3 wherein the control input is to cause a change in the current mode, wherein the host  
4 processor is to create the first logical connection if the current mode of the apparatus  
5 is the storage mode, the host processor to create the second logical connection if the  
6 current mode of the apparatus is an image processing mode.

1 16. The apparatus of claim 15, wherein the host processor is to update  
2 microcode in the first programmable processor and the second programmable  
3 processor if the control input is to cause a change from the current mode.

1 17. The apparatus of claim 16, wherein the control input to cause the current  
2 mode to be the storage mode is a pause operation of display of the video on a  
3 display of the video display device.

1 18. The apparatus of claim 16, wherein the control input to cause the current  
2 mode to be the storage mode is a rewind operation of display of the video on a  
3 display of the video display device.

1 19. A system comprising:  
2 a video tuner to receive a signal, wherein the video tuner is to extract an  
3 analog video signal at a frequency from the signal;  
4 a video signal processor to receive the analog video signal and to convert the  
5 analog video signal to a digital video signal;  
6 a double data rate (DDR) random access memory (RAM); and  
7 a programmable processing unit having at least one programmable processor  
8 and a host processor, wherein the host processor is to configure the at least one  
9 programmable processor to compress and store the digital video signal in the DDR  
10 RAM if the system is in a storage mode, and wherein the host processor is to  
11 configure the at least one programmable processor to perform at least one image  
12 processing operation if the system is in an image processing mode.

1 20. The system of claim 19, wherein the at least one programmable processor is  
2 to perform the at least one image processing operation across multiple frames of the  
3 digital video signal.

1 21. The system of claim 19, wherein a first programmable processor of the at  
2 least one programmable processor is to store results of a first image processing  
3 operation of the at least one image processing operation in the DDR RAM and  
4 wherein a second programmable processor of the at least one programmable  
5 processor is to retrieve the results from the DDR RAM and is to perform a second  
6 image processing operation of the at least one image processing operation.

1 22. The system of claim 19, wherein the at least one image processing operation  
2 is selected from a group consisting of a ghost reduction operation, a temporal noise  
3 reduction operation and a spatial noise reduction operation.

1 23. A machine-readable medium that provides instructions, which when  
2 executed by a machine, cause said machine to perform operations comprising:  
3 receiving video into a video display device;  
4 storing, by at least one processor, the video into a memory, upon  
5 determining that the video display device is in a storage mode; and  
6 performing enhanced image processing on the video with the at least one  
7 processor, upon determining that the video display device is in an image processing  
8 mode.

1 24. The machine-readable medium of claim 23, further comprising compressing,  
2 by the at least one processor, the video prior to storing the video into the memory,  
3 upon determining that the video display device is within the storage mode.

1 25. The machine-readable medium of claim 24, wherein compressing, by the at  
2 least one processor, the video comprises performing frame reduction on the video,  
3 by a first processor of the at least one processor.

1 26. The machine-readable medium of claim 25, wherein compressing, by the at  
2 least one processor, the video comprises scaling, by a second processor of the at  
3 least one processor, of the video.

1 27. The machine-readable medium of claim 23, wherein performing enhanced  
2 image processing on the video comprises performing a ghost reduction operation.

1 28. The machine-readable medium of claim 23, wherein performing enhanced  
2 image processing on the video comprises performing a noise reduction operation.

1 29. The machine-readable medium of claim 23, wherein performing enhanced  
2 image processing on the video with the at least one processor comprises performing  
3 a first enhanced image processing operation on the video with a first processor of  
4 the at least one processor and performing a second enhanced image processing  
5 operation on the video with a second processor of the at least one processor.

1 30. The machine-readable medium of claim 29, further comprising transmitting  
2 output of the first enhanced image processing operation from the first processor to  
3 the second processor through a logical connection that includes a path through a  
4 third processor, wherein the third processor is not configured to perform a process  
5 operation on the output as part of the transmitting of the output through the logical  
6 connection.